A Prototype Low-Noise Sixty-Four Channel Readout Card for the PHENIX Muon Tracker Cathode Strip Detector Subsystem

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Abstract

The development and test results of a prototype sixty-four channel readout card with emphasis on the eight-channel preamplifier/shaping amplifier ASIC [1] design and performance are presented.

Design objectives for the preamplifier include; less than 3000 electrons (rms) of noise for 150 pF of detector capacitance, integration time of 700 ns to 1 us over the range of detector capacitance values from 10 pF to 250 pF, return to baseline of less than 100 us, gain of about 3.5 mV/fC and 11 bits of dynamic range. The nominal power consumption is about 70 mA at a supply voltage of 5V.

The readout card design integrates eight of the preamplifier ASICs and two thirty-two channel AMU/ADC [2] (Analog Memory Unit/Analog to Digital Converter (12-bit)) ASICs onto a 6U format printed circuit board. Both ASICs were designed at Oak Ridge National Laboratory while the readout card was designed at Los Alamos National Laboratory.

I. INTRODUCTION

The Muon Tracker Detector subsystem of the PHENIX program requires a total of 50,000 channels of detector front-end electronics for the Cathode Strip Detectors.

The readout electronics will be located inside of the Muon Tracker magnet where space is very limited. The front-end electronics will be connected to the detectors with a minimum cable length of 50 cm.

A low-noise multi-channel preamplifier/shaper ASIC was required to meet the space and power constraints imposed by the mechanical geometry of the detector design and to obtain the required physics results. The stringent space constraints also require a minimum of sixty-four channels for each front-end electronics readout card.

The geometry and size of the cathode strip detectors imposes a wide range of detector capacitance load values, 10 pF to 250 pf. The longest cathode strip is approximately 4 meters long.

II. 8 CHANNEL PREAMPLIFIER/SHAPER

A. Requirements

An integrated preamplifier/shaping ASIC was designed to meet the stringent physics requirements and mechanical constraints. Extremely limited access to the front-end electronics requires remote control of the ASIC through digital serial control. Serial control requirements include individual channel masking (reset), pulse testing capability and the ability to adjust the output bias level. The ASIC was designed to operate on a single +5V supply to simplify the entire readout electronics design and minimize power consumption.

The chip was packaged in a 100 pin Quad Flat Pack with signal and signal return inputs on one side and signal outputs on the opposite side of the chip to simplify routing and minimize crosstalk and feedback from the outputs to the inputs. The chip requires digital and analog power and ground connections.

B. Serial Control

The ASIC can be loaded with a 34-bit serial string to set up the operating parameters and functions of the ASIC or the ASIC can be operated with the power up defaults. The 34-bit serial string consists of the following: 6 bits for each of the three internal DACs (all eight channels are controlled by a single DAC), 8 bits for individual channel masking (reset), 8 bits for individual channel control of internal pulse injection. (Figure 1) The internal DAC functions are as follows: amplitude control of injection test pulse, output DC level control, feedback resistor value of the preamplifier. The ASIC can also be controlled with an adjustable external analog voltage reference to bias the two shaping stages. This works in conjunction with the internal Offset DAC to control the output DC level. The nominal output DC level for the ASIC is 4-4.5 V utilizing a 5 V supply to obtain maximum dynamic range.

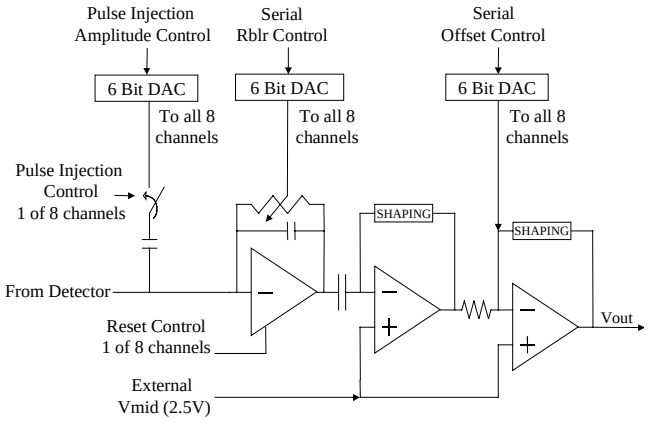

Figure 1: Block Diagram of one channel of 8 channel preamplifier/shaping ASIC with external serial controls

C. Operation

The ASIC was tested extensively on a test board explicitly designed to test all eight channels at once on a single chip. A PC interface for serial control and data acquisition was designed into the board. A nominal range of values for the external serial control was determined that would operate the chip to meet the requirements of the Muon Tracker detector system.

To meet the dynamic range requirements, 0.8 fC to 800 fC, (11 bits) with a nominal gain of 3.5 mV/fC, a nominal output DC voltage of ~4 V is required. The maximum swing of the ASIC is 3 V below the offset. The linearity degrades if the signal swings below the 1 V level. A swing of 2.8 V is required for 800 fC.

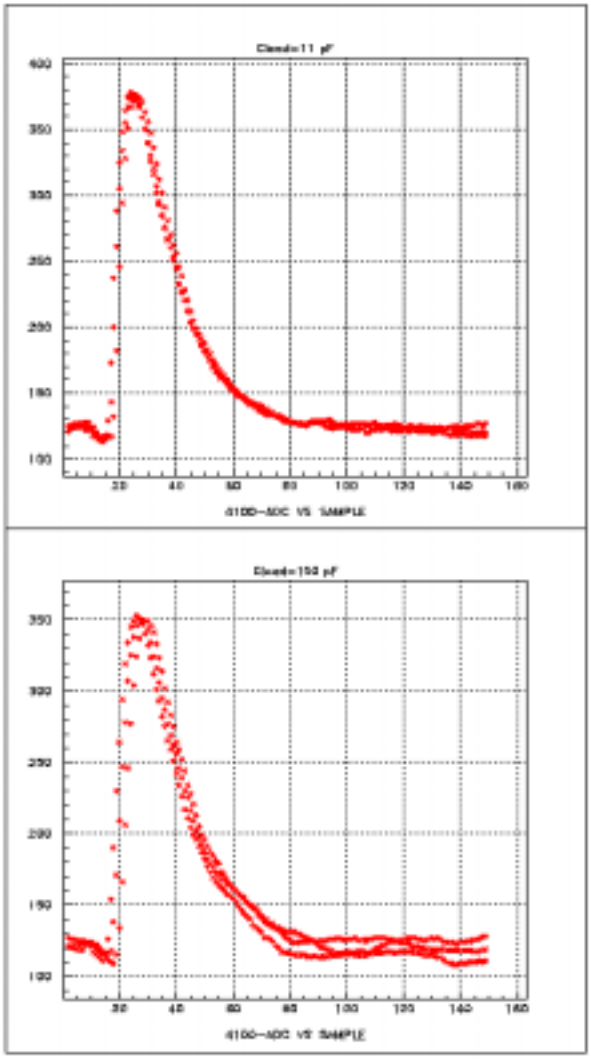

Figure 2: Sample waveforms for detector capacitance values of 11 pF and 100 pF

The amplitude of the signal was measured for a range of detector capacitance values. Figures 2 and 3 show plots of three sample waveforms for each of three detector capacitance values, 11 pF, 100 pF and 185 pF. The plots show inverted waveforms with the vertical scale in ADC counts, 1mV/count. The gain decreased from 3.5mV/fC at 0 pF to 2.75mV/fC at 185 pF.

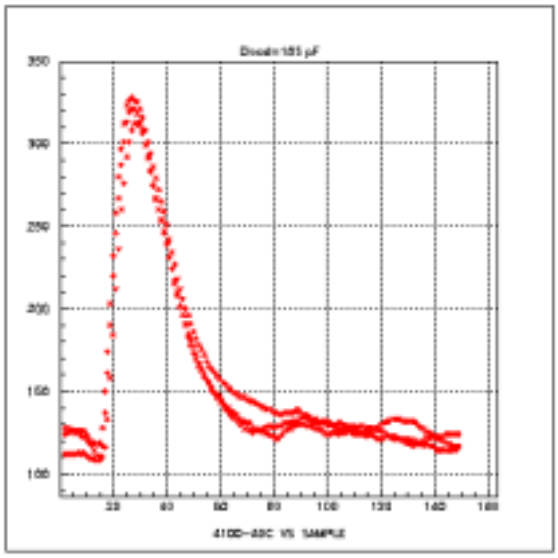

Figure 3: Sample waveforms for detector capacitance value of 185 pF

The performance was determined to be acceptable and the next step was to incorporate the chips into a prototype 64 channel front-end electronics module.

III. Prototype Readout Electronics Card (ROC)

The readout electronics card integrates eight of the eight-channel preamplifier/shaper ASICs and two thirty-two channel AMU/ADC ASICs onto a 6U form factor printed circuit board.

The detector signals are pseudo-differential with a signal and signal return pair for each cathode strip to each channel of the preamplifier. The serial control string for the ASICs is daisy chained through all eight ASICs.

The noise performance of the ROC is extremely critical for the success of the Muon Tracker subsystem. This implies extremely careful layout of the printed circuit board with both analog and digital power and grounds required by the preamplifier ASIC to maintain a very low noise level.

A. Design

The analog input lines are very sensitive to the surrounding signals so the layout of the input lines is extremely critical for optimal noise performance. A total of 128 signal and signal return lines are required from the detector into one ROC plus eight additional signal return and detector frame ground lines. Digital control lines from the backplane are required to control the AMU/ADC and associated circuitry. A single connector was used for the analog signal and signal return lines from the detector and a separate connector was used for all other lines into the module. The analog lines were not connected to the

backplane. They were simply passed through a header to the detector cables.

All signal and signal return lines to the ASIC require AC coupling. The signal return is referenced to the supply voltage and is greater than 0 V. The signal lines are also greater than 0 V. The analog lines were embedded between ground planes to shield the lines from possible EMI sources. The board is shown in figure 4. The analog section showing only the preamplifiers is shown in figure 5.

The ASICs require extensive power supply decoupling for optimum performance. This is often overlooked in low noise designs. The preamplifier has four power supply requirements. Digital (3 pins), shaper (4 pins), Vmid (2 pins) and Preamplifier (1 pin). The preamplifier supply is the most critical and requires an additional large valued tantalum capacitor (22 uF-50 uF) to meet the noise requirements. All others require a 0.1 uF and a tantalum in the range of 1 uF-10 uF.

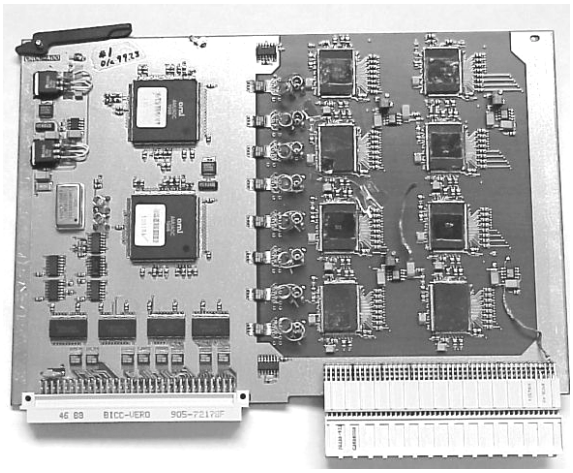

Figure 4: Front End Electronics Readout Card for Cathode Strip Detector (9.187" x 6.299" (233.35 mm x 160 mm))

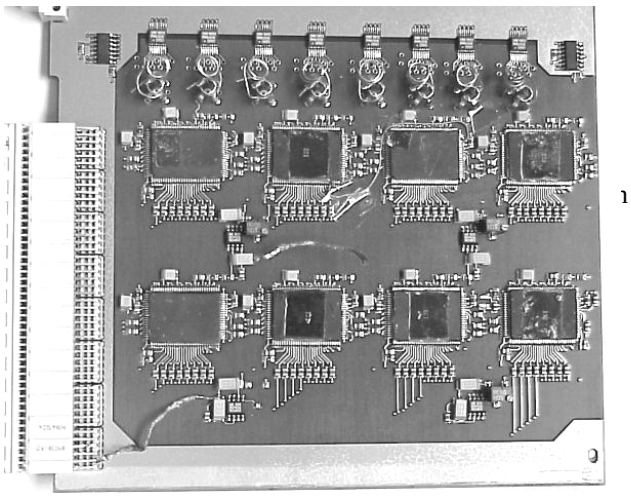

Figure 5: Front End Electronics Readout Card, analog section showing eight 8-channel preamplifier/shaping ASICs

B. Performance

The ROC was connected to the test board previously used to test the ASICs to load the serial string and test the analog section. A 32 kHz crystal and a 200 MHz PECL oscillator are always running on the board.

The noise and gain were measured with the output offset set for approximately 4 V and the BLR setting for minimum overshoot, but optimum return to baseline (this affects the gain of the amplifier), with and without the detector and cables.

1) Without detector and cables

The gain was measured using a 1% injection capacitor with a precision pulser over a range of input levels. The maximum gain variation was 1-2% for the channel. The gain varied between 3.5 mV/fC and 4.1 mV/fC over all eight chips.

The noise was measured and the rms level was between 550 μV and 650 μV (about 1150 electrons using 3.5 mV/fC). The specified noise level is about 1200 electrons so this is within the specifications. (Figure 6)

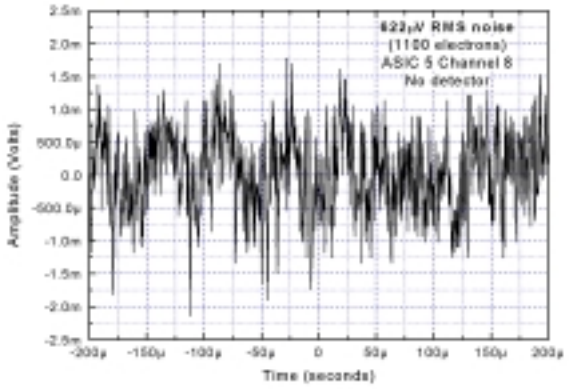

Figure 6: Noise of a typical channel of one without cables or detector

2) With detector and cables

The cable length used in the tests was 24 inches with 17 twisted pair and an overall shield. The prototype detector is about six feet tall with a capacitance in the range of 150 pF. The gain with the detector and cables decreased by about 20% but the gain variation remained the same as measured previously. This is consistent with the tests of the ASIC using the test board.

The noise was measured to be between 1.7 mV and 3 mV depending on the position of the ASIC on the board (noise increased due to layout). When an additional 50 uF tantalum capacitor was added to the preamplifier supply, the noise remained very consistent on all chips at about 1.7 mV to 1.8 mV rms (3400 electrons, 3.3 mV/fC, 3800 electrons, 2.8 mV/fC). The requirements are 3000 electrons at 150 pF so this is high, but reasonable for a first round prototype.

IV. Conclusion

A first round prototype 64 channel read-out-card has been designed and the analog section tested. The performance is very close to meeting the requirements. Additional testing needs to be finished on the data acquisition section of the read-out-card, but this requires the controller card that is currently being completed. A completed chassis will include 4 ROCs and two controller cards for 256 channels.

V. Acknowledgments

Other major contributors to the design of the ROC include Gary Smith and Gary Richardson of Los Alamos National Laboratory for the layout of the board. Melynda Brooks helped setup the CAMAC system to acquire the data and PAW to analyze the data when the chips were being tested.

VI. References

[1] M.S. Emery, et al., “Muon Tracker Preamp User’s Data Sheet” *Oak Ridge National Laboratory, December 1998*

[2] M.S. Emery, et al., "A Multi-Channel ADC for Use in the PHENIX Detector," *IEEE Trans.* Nucl. Sci., Vol. 44, pp.374-378, June 1997.